CS 2420 Lab 7

Topics: Latches and Flip-Flips from NAND Gates

Pre Lab: Fill in all the expected values for T1-T3. Be able to explain what a pull up/down resistor does.

T1. S\R\ latch from coupled NAND gates.

Using a 7400 quad 2-input NAND gate chip, construct the circuit shown in the right figure. Now close the switches, with S\ and R\ initially connected to logic 1 as shown. Then record the values of Q and Q\ as S\ and R\ go through the indicated changes:

| Input | | Observe | d Output | Expected Output | |
|-------|----|---------|----------|-----------------|----|
| S\ | R\ | Q | Q\ | Q | Q\ |
| 1 | 0 | | | | |
| 1 | 1 | | | | |
| 0 | 1 | | | | |
| 1 | 1 | | | | |
| 1 | 0 | | | | |
| 0 | 0 | | | | |
| 0 | 1 | | | | |



T2. SR Latch with Enable

This variant of the latch has a control input E that enables the response of the latch to the settings of the SR inputs. When E=0 there should be no change in Q and Q\ no matter what happens to S and R. When E=1 the latch sets when S=1 and R=0 and resets when S=0 and R=1. Note that the design has the effect of making the set-reset inputs both active high. Continue measuring the outputs Q and Q/ in response to the SR inputs and the control signal E.

| Input | | | Observed Output | | Expected Output | |
|-------|---|---|-----------------|----|-----------------|----|
| Е | S | R | Q | Q\ | Q | Q\ |
| 0 | 0 | 0 | | | | |
| 0 | 1 | 0 | | | | |
| 0 | 1 | 1 | | | | |
| 0 | 0 | 1 | | | | |
| 1 | 0 | 1 | | | | |
| 1 | 0 | 0 | | | | |
| 1 | 1 | 0 | | | | |
| 1 | 1 | 1 | | | | |
| 1 | 0 | 1 | | | | |
| 1 | 0 | 0 | | | | |



T3. D-latch with pull-up resistor

This circuit implements a D latch with pullup resistor so that the default state of the latch is logic l; i.e., the latch is set. The resistance of the pullup resistor should be a few thousand ohms. The purpose of the pullup resistor in this case is to give a default state to the latch independent of the data input setting. Now complete the following table of observations:

| Input | Observe | d Output | Expected Output | | |
|-------|---------|----------|-----------------|----|--|
| D | Q | Q\ | Q | Q\ | |
| 0 | | | | | |
| 1 | | | | | |
| 0 | | | | | |
| Ζ | | | | | |



T4. Build a circuit with flipflops.

Consider the schematic diagram below. The D flipflops are positive edge triggered with Set and Reset pins. The flipflops are configured to be a counter. The device in the upper right corner is a hex display. Use DSCH to build such a counter. Note that both flipflops receive the same clock pulse. After your instructor has verified your circuit works, take screen shot(s) for your report. Be sure you are able to explain what the counter sequence is.

